IN THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Original) A semiconductor device comprising: a semiconductor substrate of a first conductivity type wherein an element isolation region is formed; a gate electrode formed above the semiconductor substrate with a gate insulating film placed therebetween; a sidewall spacer, made of an insulating film, arbitrarily formed on the sidewall of the gate electrode; a drift region of a second conductivity type provided with a low concentration region formed in the semiconductor substrate under, at least, one edge side in the channel length direction of the gate electrode; a high concentration region of the second conductivity type surrounded by the drift region, with the exception of the low concentration region; an interlayer insulating film formed over the entire surface of the semiconductor substrate; and a contact hole as well as a metal wire formed in a predetermined portion,

wherein the drift region of the second conductivity type provided with the low concentration region is a region formed by means of impurity ion implantation with predetermined implantation angles respect to a surface of the semiconductor substrate and with four different directions.

2. (Original) A semiconductor device of claim 1, wherein the semiconductor substrate has a trench formed by means of etching using a mask constituted the gate electrode and the sidewall spacer arbitrarily formed, and the drift region and the high concentration region are formed in the trench.

3. (Original) A semiconductor device of claim 1, wherein the drift region of the second conductivity type provided with a low concentration region is formed on both ends in the channel length direction of the gate electrode, and the high concentration regions of the second conductivity type are formed as a source region and a drain region in the drift region with the exception of the low concentration region.

4. (Original) A semiconductor device of claim 2, wherein the implantation angle is from 30° to 70°.

5. (Original) A semiconductor device of claim 1, wherein the four different directions are directions wherein a first direction is a direction parallel to the channel width direction and the other three directions have incident angles of 90°, 180° and 270°, respectively, relative to the first direction.

6. (Original) A manufacturing method for a semiconductor device comprising the step of:

forming a gate electrode via a gate insulating film above a semiconductor substrate of a first conductivity type, wherein an element isolation region is formed;

arbitrarily forming sidewall spacers, made of a insulating film, on the sidewalls of the gate electrode;

forming a drift region of a second conductivity provided with a low concentration region in the semiconductor substrate under, at least, one edge side in the channel length direction of the gate electrode by means of impurity ion implantations with predetermined implantation angles respect to a surface of the semiconductor substrate and with four different directions;

forming a resist pattern and forming a high concentration region of the second conductivity type surrounded by the drift region, with the exception of the low concentration region, using the resist pattern;

removing the resist pattern and forming an interlayer insulating film over the entire surface of the semiconductor substrate; and

forming a contact hole in predetermined portion and forming a metal wire.

7. (Original) A manufacturing method for a semiconductor device comprising the step of:

forming a gate electrode via a gate insulating film above a semiconductor substrate of a first conductivity type, wherein an element isolation region is formed;

arbitrarily forming sidewall spacers, made of an insulating film, on the sidewalls of the gate electrode;

forming a trench by etching the semiconductor substrate using a mask constituted the gate electrode and the sidewall spacer arbitrarily formed

forming a drift region of a second conductivity type provided with a low concentration region in the semiconductor substrate under, at least, one edge side in the

channel length direction of the gate electrode by means of impurity ion implantation with predetermined implantation angles respect to a surface of the semiconductor substrate and with four different directions;

forming a resist pattern and forming a high concentration region of the second conductivity type surrounded by the drift region, with the exception of the low concentration region, using the resist pattern;

removing the resist pattern and forming an interlayer insulating film over the entire surface of the semiconductor substrate; and

forming a contact hole in predetermined portion and forming a metal wire.

8. (Currently Amended) A manufacturing method for a semiconductor device of claim 6 ~~or 7~~, wherein the implantation angle is from 30° to 70°.

9. (Currently Amended) A manufacturing method for a semiconductor device of claim 6 ~~or 7~~, wherein the drift region of the second conductivity type provided with a low concentration region is formed on both ends in the channel length direction of the gate electrode, and the high concentration regions of the second conductivity type are formed as a source region and a drain region in the drift region with the exception of the low concentration region.

10. (Currently Amended) A manufacturing method for a semiconductor device of claim 6 ~~or 7~~, wherein the four different directions are directions wherein a first direction is a direction parallel to the channel width direction and the other three directions have incident angles of 90°, 180° and 270°, respectively, relative to the first direction.

11. (New) A manufacturing method for a semiconductor device of claim 7, wherein the implantation angle is from 30° to 70°.

12. (New) A manufacturing method for a semiconductor device of claim 7, wherein the drift region of the second conductivity type provided with a low concentration region is formed on both ends in the channel length direction of the gate electrode, and the high concentration regions of the second conductivity type are formed as a source region and a drain region in the drift region with the exception of the low concentration region.

13. (New) A manufacturing method for a semiconductor device of claim 7, wherein the four different directions are directions wherein a first direction is a direction parallel to the channel width direction and the other three directions have incident angles of 90°, 180° and 270°, respectively, relative to the first direction.